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**NEW QUESTION: 1** Which of the following is a set of data processing elements that increases the performance in a computer by overlapping the steps of different instructions?  
**A.** reduced-instruction-set-computer (RISC) **B.** pipelining **C.** complex-instruction-set-computer (CISC) **D.** multitasking  
**Answer: B**  
**Explanation:** Pipelining is a natural concept in everyday life, e.g. on an assembly line. Consider the assembly of a car: assume that certain steps in the assembly line are to install the engine, install the hood, and install the wheels (in that order, with arbitrary interstitial steps). A car on the assembly line can have only one of the three steps done at once. After the car has its engine installed, it moves on to having its hood installed, leaving the engine installation facilities available for the next car. The first car then moves on to wheel installation, the second car to hood installation, and a third car begins to have its engine installed. If engine installation takes 20 minutes, hood installation takes 5 minutes, and wheel installation takes 10 minutes, then finishing all three cars when only one car can be assembled at once would take 105 minutes. On the other hand, using the assembly line, the total time to complete all three is 75 minutes. At this point, additional cars will come off the assembly line at 20 minute increments. In computing, a pipeline is a set of data processing elements connected in series, so that the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time-sliced fashion; in that case, some amount of buffer storage is often inserted between elements. Pipelining is used in processors to allow overlapping execution of multiple instructions within the same circuitry. The circuitry is usually divided into stages, including instruction decoding, arithmetic, and register fetching stages, wherein each stage processes one instruction at a time. The following were not correct answers: CISC: is a CPU design where single instructions execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store) within a single instruction. RISC: is a CPU design based on simplified instructions that can provide higher performance as the simplicity enables much faster execution of each instruction. Multitasking: is a method where multiple tasks share common processing resources, such as a CPU, through a method of fast scheduling that gives the appearance of parallelism, but in reality only one task is being performed at any one time. Reference: KRUTZ, Ronald L. & VINES, Russel D., The CISSP Prep Guide: Mastering the Ten Domains of Computer Security, pages 188-189. Also see [http://en.wikipedia.org/wiki/Pipeline\\_\(computing\)](http://en.wikipedia.org/wiki/Pipeline_(computing))

**NEW QUESTION: 2** During a post-mortem meeting, discussions come up who has to take responsibility for some major failures. It has become obvious that the attendees of the meeting will not come to a jointly accepted conclusion. What is not an appropriate strategy for such a situation?  
**A.** Insist on objective criteria and standards **B.** Suspend this discussion and schedule another meeting **C.** Separate the people from the problem **D.** Focus on interests, not positions  
**Answer: B**

**NEW QUESTION: 3** A list report includes columns for purchase requests and regional cost

centers. A manager wants the report to show the total number of purchase requests for each of the regional cost centers. How do you configure the report definition? **A.** Filter the results so that the report includes only cost center and purchase requests. **B.** Summarize the purchase requests column by count. **C.** Use the purchase requests column to group the cost centers. **D.** Summarize the regional cost centers by count. **Answer: B**

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